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Seventh Semester B.E. Degree Examination, July/August 2022
VLSI Circuits and Design

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting atleast TWO questions from each part.

PART – A

- 1 a. Explain the evolution of VLSI technology with respect to Moore's law. (08 Marks)
- b. Explain the working of nMOS enhancement type transistor for different regions of operation and draw its input and output characteristics. (12 Marks)
- 2 a. With relevant diagrams, explain the N-well CMOS fabrication process. (10 Marks)
- b. Show that the pull-up and pull-down ratio of nMOS inverter driving another nMOS inverter is 8:1. (10 Marks)
- 3 a. Explain the working of a CMOS inverter in different regions of operation with the help of transfer characteristics. (10 Marks)
- b. Explain about latch up in CMOS circuits, what are the remedies to avoid latch up? (10 Marks)
- 4 a. How will you represent wires, transistors and contact acts considering lambda based design rules? (08 Marks)
- b. Draw the transistor level diagram and stick diagram of two way selector. (06 Marks)
- c. Draw the layout of two point nMOS NOR gate. (06 Marks)

PART – B

- 5 a. Explain the operation of inverting and Non-inverting super buffers. (08 Marks)
- b. Define the scaling factor for i) gate area ii) gate capacitance iii) gate delay iv) channel resistance v) maximum operating frequency vi) saturation current. (12 Marks)
- 6 a. Explain about Dynamic CMOS logic, How can it be improved for cascading of logic structures. (10 Marks)
- b. Explain the bus arbitration logic and draw its stick diagram. (10 Marks)
- 7 a. Implement a 4-way multiplexer with nMOS switches and explain how can it be designed to operate as logic gates. (10 Marks)
- b. Design a 4-bit adder element and implement the function of ALU with it. (10 Marks)
- 8 Write a short note on the following :
 - i) E-beam masks (05 Marks)
 - ii) Pass transistor logic (05 Marks)
 - iii) Sheet resistance (05 Marks)
 - iv) Pseudo nMOS logic. (05 Marks)

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